



In-depth Analysis of Hardware Loop Testing Method: Design, Implementation, and Applications

Priyank Jayantilal Rathod¹, Anurag²

Intel Corporation, Folsom, CA

Email id: ¹rathodpriyank@gmail.com, ²anurag.nndn@gmail.com

Abstract Hardware testing is essential to any electronic system development life cycle. It ensures the functionality, reliability, and quality of the hardware components involved in any device. Among various hardware testing methods, loop testing has gained significant attention due to its ability to test a large portion of the digital circuitry systematically and efficiently. The technique involves creating a loop that simulates the expected operating conditions of the hardware component and then testing it under those conditions to verify its performance. This article will provide an in-depth analysis of the hardware loop testing method, including its design, implementation, and applications. Hardware loop testing is an essential part of the hardware testing process, which involves verifying the functionality and performance of hardware components by subjecting them to various test cases.

Keywords Testing, Embedded Systems, Real-Time, Control Systems, Computational Modeling, Feedback loop

Introduction

Hardware testing is an integral part of any electronic system development process. It ensures that the designed hardware components meet the specified functional and performance requirements. Various hardware testing methods exist to cater to different testing needs. Among these, loop testing stands out due to its efficiency in systematically testing a large portion of digital circuitry. In this section, we will introduce the concept of loop testing and discuss why it is essential for hardware development. Loop testing is a methodology for testing digital logic circuits. It derives its from the test vector loops generated during testing. This technique primarily aims to test multiple logic gates or combinational blocks in a loop instead of individually. The loop includes the input vectors that activate all the logic gates under test and output vectors that check the resulting outputs against expected values.

Designing loop tests:

Designing loop tests requires careful planning and consideration to ensure comprehensive testing coverage. The design of hardware loop testing expects behavior under different operating conditions. The next step is to create a test bench to simulate these operating conditions using a combination of analog and digital circuits. J. Park et al. have studied to establish a development environment for ECU RCP (rapid control prototyping), which can help develop ECUs to be installed in next-generation vehicles [1].

It would help the ECUs by using a model-based design process. It would significantly reduce the cost and provide flexibility for the ECU development process. Similarly, M. Kaczmarek et al. have provided the results for SoC solutions for designing the hardware solutions [2]. Hence, developing the systems for loop testing can be used in various areas. Many steps are involved in creating such systems, listed here sequentially. Identifying the requirements of the hardware component consists of determining the input and output signals and the



expected behavior under different operating conditions. After gathering the requirements, the test vectors are created to activate all the logic gates that check their correct functioning under test and output vectors. This may involve using a truth table or Boolean algebraic expressions to generate valid inputs and expected outputs. The test bench is responsible for simulating the operating conditions of the hardware component using a combination of analog and digital circuits. Once the test vectors are defined and aligned with the system requirement, the test bench interface is created between the Digital Under Test (DUT) and the testing equipment. The test bench should include necessary interfaces, clocks, and control signals. Test cases are designed to verify the functionality and performance of the hardware component under various operating conditions. In the final stage, once the system is ready, any simulator software, either created and tailored for the application or generalized software, is used to verify the functionality of the test vectors and the expected results before actual hardware testing. This step ensures that the design is correct and free from logical errors. After running the test cases, the results are validated to ensure that the hardware component functions correctly and performs as expected. F. Shanqiang et al. have performed the function verification and performance evaluation test of all secondary devices, networks, switches, merge cells, smart/ terminals, protections, monitoring, measurement, and recording equipment, where building the hardware platform is explored [3]. F. Gao et al. designed hardware and software-based systems to solve the Hardware Loop simulation [4].

Implementing Loop Tests

After designing loop tests, it's time to implement them practically to validate them. Implementing a hardware loop testing method involves creating a physical test bench that can simulate the operating conditions of the hardware component. L. S. Prabhu et al. have implemented a feedback loop system for a mixed-signal VLSI test system using an embedded digital signal processing (DSP) unit that provides superior flexibility in device testing applications [5]. The loop typically has analog and digital circuits, such as voltage regulators, current sources, and logic gates. The test bench must be designed to accurately simulate the hardware component's expected operating conditions, including temperature and humidity variations—other environmental factors. Implement the loop test and the required hardware components, including the DUT, test equipment, power supplies, and interconnecting wires. Connecting them to the designed test bench and all interfaces and control signals to tune the test parameters. Once all the steps are validated, the output of the DUT signals is recorded against the expected results over the test time to evaluate the test results. J. Keranen et al. are testing a Model-based testing (MBT) in a hardware-in-the-loop (HIL) platform, a simulation and testing environment for embedded systems, in which test design automation provided by MBT is combined with HIL methodology [6].

Applications and Benefits of Loop Testing

Hardware loop testing has system-level applications for testing the device against rapid prototyping. It is used in design verification where logic related to the design with the blocks can be tested in line with the whole system or a separate block. Identifying the faults in a separate block or the entire system where they can be detected in the earlier design would help the designers. Understand the overall system. The system can detect the difference between the delay between the physical testing and the HIL system, where the results can be compared in real-time and match the actual vs. the expected results of any system. A. Rothstein et al. have found a novel approach to perform the software implementation of the HIL and validate against the physical results from the test bench to validate the close gap between the software base a hardware-based tools and methods used in the HIL [7].

Hardware loop testing is essential to test any system in production. It is utilized in customer electronics, too, over the test time to evaluate the test functionality and verify the device before reaching the masses for tablets, mobile phones, or laptops.

The hardware loop testing method offers several benefits, such as improving reliability before problems occur. J. C. V. S Junior et al. present the testing of real-time embedded applications using hardware-in-loop simulation methods [8]. HIL would reduce development costs as issues can be identified and resolved early in the design process. It also means that the systems getting shipped are safe and reliable before they become a significant problem in the field.



Challenges and Limitations of Loop Testing

While loop testing offers many benefits, it has specific challenges and limitations. D. Matthes et al. use mixed signal devices and describe how to read the CMOS channel, which involves many challenges and solutions around it [9]. Designing and implementing a comprehensive loop test for large digital circuits can be challenging due to the many logic gates and combinational blocks involved. It is time-consuming as these loop tests can take time, especially when testing large circuits with numerous inputs and outputs. HIL Requires extensive planning: Proper planning is essential for loop testing to ensure comprehensive test coverage, which can be complex and time-consuming. P. Bernardi et al. have described a low-cost approach to develop such a system, but most of these systems are expensive, and it becomes one of the bottlenecks as it brings the upfront cost [10].

Conclusion

Loop testing is an essential methodology in hardware development to test digital logic circuits systematically and efficiently. By understanding loop test design, implementation, and applications, engineers can create high-quality electronic systems that meet their specified requirements while ensuring robustness, reliability, and functionality. Despite its challenges, loop testing's benefits far outweigh its limitations, making it a critical tool in modern hardware development.

Hardware loop testing is a vital part of the hardware testing process and involves simulating the expected operating conditions of a hardware component to verify its functionality and performance. The method consists in creating a test bench that can simulate these operating conditions using a combination of analog and digital circuits and running test cases on the test bench to validate the results. Hardware loop testing has various applications in various industries, including semiconductor manufacturing, aerospace, automotive, medical devices, and consumer electronics. The benefits of hardware loop testing include improved reliability, reduced costs, faster time-to-market, improved performance, and increased safety. Using the hardware loop testing method; engineers can ensure that their designs are safe, reliable, and meet the required specifications before being deployed in the field.

Reference

- [1]. J. Park, B. Wang, J. Jeon and S. -H. Hwang, "Hardware in-the-loop simulation for ABS using 32-bit embedded system," 2011 11th International Conference on Control, Automation and Systems, Gyeonggi-do, Korea (South), 2011, pp. 575-580.
- [2]. M. Kaczmarek and P. Koralewicz, "Hardware in the loop simulations of industrial application using system on the chip architecture," 2016 International Conference on Signals and Electronic Systems (ICSES), Krakow, Poland, 2016, pp. 157-160, doi: 10.1109/ICSES.2016.7593842.
- [3]. F. Shanqiang, H. Aijun, H. Jie and Yangyingan, "Hardware Platform Design for Network Performance Closed-Loop Testing System of Smart Substations," 2014 7th International Conference on Intelligent Computation Technology and Automation, Changsha, China, 2014, pp. 288-291, doi: 10.1109/ICICTA.2014.77.
- [4]. F. Gao and F. Deng, "Design of a Networked Embedded Software Test Platform Based on Software and Hardware Co-simulation," 2016 IEEE International Conference on Software Quality, Reliability and Security Companion (QRS-C), Vienna, Austria, 2016, pp. 375-381, doi: 10.1109/QRS-C.2016.57.
- [5]. L. S. Prabhu and D. A. Rosenthal, "A DSP-based feedback loop for mixed-signal VLSI testing," Proceedings International Test Conference 1997, Washington, DC, USA, 1997, pp. 670-674, doi: 10.1109/TEST.1997.639679.
- [6]. J. Keränen and T. Rätty, "Validation of Model-Based Testing in Hardware in the Loop Platform," 2013 10th International Conference on Information Technology: New Generations, Las Vegas, NV, USA, 2013, pp. 331-336, doi: 10.1109/ITNG.2013.53.
- [7]. A Rothstein, L. Siekmann and V. Staudt, "Combined-Hardware-in-the-Loop system and its test-bench verification," 2017 International Conference on Optimization of Electrical and Electronic Equipment



- (OPTIM) & 2017 Intl Aegean Conference on Electrical Machines and Power Electronics (ACEMP), Brasov, Romania, 2017, pp. 581-586, doi: 10.1109/OPTIM.2017.7975031.
- [8]. J. C. V. S. Junior, A. V. Brito and T. P. Nascimento, "Testing Real-Time Embedded Systems with Hardware-in-the-Loop Simulation Using High Level Architecture," 2015 Brazilian Symposium on Computing Systems Engineering (SBESC), Foz do Iguacu, Brazil, 2015, pp. 142-147, doi: 10.1109/SBESC.2015.34.
- [9]. D. Matthes and J. Ford, "Technique for testing a very high-speed mixed signal read channel design," Proceedings International Test Conference 2000 (IEEE Cat. No.00CH37159), Atlantic City, NJ, USA, 2000, pp. 965-970, doi: 10.1109/TEST.2000.894308.
- [10]. P. Bernardi and L. Ciganda, "An Adaptive Low-Cost Tester Architecture Supporting Embedded Memory Volume Diagnosis," in IEEE Transactions on Instrumentation and Measurement, vol. 61, no. 4, pp. 1002-1018, April 2012, doi: 10.1109/TIM.2011.2179822.

