Available online www.jsaer.com

***Journal of Scientific and Engineering Research*, 2021, 8(11):13-23**

Research Article

ISSN: 2394-2630
CODEN(USA): JSERBR

Dual-Buck Structure Embedded Three-Switch Legs for Multi-Port Power Converters

Bang Le Huy Nguyen[1], Viet-Hong Tran[2,*]

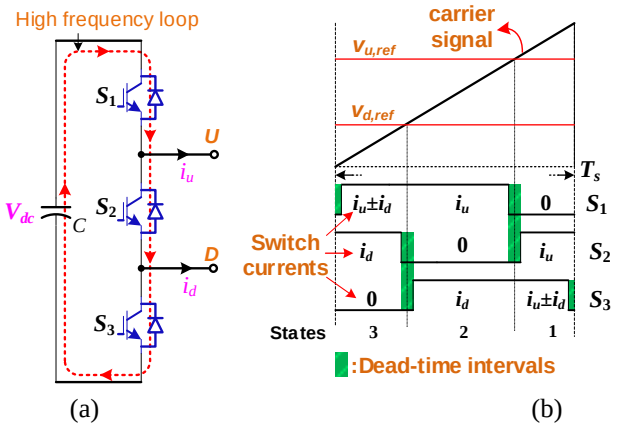
[1]Department of Electrical and Computer Engineering, Clarkson University, NY, US
[2]Department of Mechatronics Engineering, Faculty of Mechanical Engineering, Ho Chi Minh city University of Technology, VNU-HCM
*Corresponding author: tvhong@hcmut.edu.vn

Abstract This paper proposes novel three-switch configurations with the dual-buck structures embedded inside to minimize the number of additional components. The proposed legs inherit all the benefits of dual-buck structure listed as: high reliability without short-circuit concerns, minimization of the PWM dead-time, using of power MOSFETs at high dc-rail without voltage reverse recovery problem. Since the switching diodes can be chosen independently with the optimal reverse recovery characteristics, the switching loss is significantly reduced. The proposed three-switch legs find applications in the multi-port power converter systems such as ac-ac converters, dual-output inverters, multi-input converters by replacing the conventional one. The operating principle and the competition of the proposed legs are presented. The experimental results of a single-phase dual-output inverter are provided, as a practical example, to prove the applicability of the proposed legs.

Keywords Dual-buck, dual-output, integrated converter nine-switch converter, reduced-switch-count converter, switching cell, three-switch leg

1. Introduction

The integrated multi-port power converters using three-switch leg have become an increasingly attractive research topic owing to the lower number of active switches required and the subsequent reduction in the number of accompanying circuits, such as the gate-driver circuit, gate-driver power supply, snubber, and switch protection circuit. Hence, the cost, weight, size, and failure probability of the entire system are reduced.



(a) (b)

Figure 1: The conventional three-switch leg (a) and its modulation scheme (b)

The three-switch leg shown in Fig. 1(a) was derived from the two-switch leg by adding one more switch to have one more terminal. Fig. 1(b) depicts the modulation scheme of three switches in the leg. To avoid short-circuit and float-terminal, there is only one switch turned off at a time. In comparison with using two two-switch legs, the three-switch have the benefits of one switch less and lower currents (i_u-i_d) flowing through switches (S_1 and S_3) when the terminal current directions are the opposite. Nonetheless, when these currents are the same in direction, the current stresses should be larger (i_u+i_d) [1]. The upper voltage reference should be larger than the lower voltage reference [1]. This condition limits the modulation indices in the dc-ac/ac-ac power conversion systems at different frequency (DF) mode [2] under 0.5 and the lower output voltage at always smaller the upper output voltage in the dc-dc power converters [3]. The three-switch leg was widely employed in the bidirectional dual-input or dual-output dc-dc converters [2], dual-output dc-ac inverters [3], ac-ac converters [4], and multi-port integrated converters for distributed generation systems [5] as shown Fig. 2.

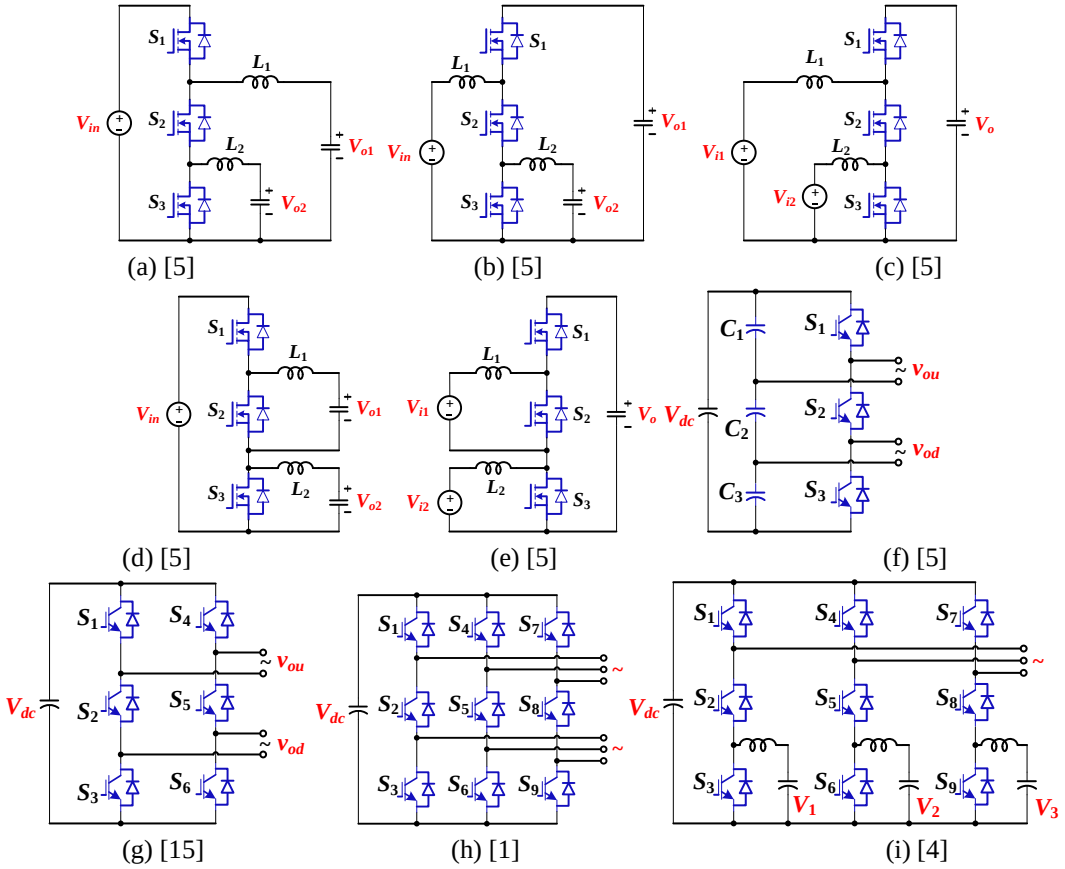


Figure 2: The integrated power converter topologies using the three-switch leg

As can be seen in Fig. 1(a), the conventional three-switch leg have the high frequency loop with three active switches connected in series. Three PWM dead-time intervals should be inserted between the switch transition to avoid short-circuit as shown in Fig. 1(b). Both power MOSFETs and IGBTs can be employed to realize the active switches. However, the power MOSFETs possess the body diodes with poor reverse recovery characteristics. The reverse current can be calculated as:

$$I_{RR} = t_F \frac{dI_F}{dt} = t_F \frac{V_{dc}}{L_{str}} \quad (1)$$

Where, t_F is the period time when the diode current goes from zero the its negative peak, L_{str} is the stray inductance of the high frequency loop, the voltage drops on the turned-off switches and the stray resistance can be neglected since they are very small compared to V_{dc}. As commonly occurs, when the dc-link voltage (V_{dc}) goes excess approximately 250 V, the reverse current during the recovery period become severe. The increase of switching losses and electromagnetic interference induced by this high reverse current become unacceptable. The soft-switching techniques with auxiliary circuits can be employed to resolve this problem. However, they

complicate power stage circuits and the control, increase the voltage and/or current stresses. The IGBT devices with better anti-paralleled diodes can displace the power MOSFETs [6]. Nonetheless, the IGBTs yield a higher switching loss and an even higher conduction loss at a certain current level due to the longer switching time and the fixed on-state forward voltage drop. Moreover, the operating frequency of the IGBTs is also typically limited to less than 20 kHz. It is much smaller than that of the power MOSFETs. As results, the control bandwidth of the converter system must be reduced, the filter requirement must be increased [7].

The patented dual-buck switching circuits [8] are an effective solution to resolve the aforementioned problems by introducing the current limiting inductors and external diodes. The dual-buck structures were widely employed for various applications in dc-dc, dc-ac, ac-dc, and ac-ac conversion systems [9]–[14]. Where, in these converters, the standard two-switch leg is displaced by the dual-buck legs. An extension of the dual-buck structure for the three-switch leg was introduced in [15] to form a dual-output inverter. However, it requires four current-limiting inductors and three external diodes, which results in the significant increase of cost and size of the converter.

This paper proposes novel dual-buck leg configurations using the minimal number of additional components. The proposed configurations possess the distinct advantages of dual-buck structure as followings.

1) The *di/dt* of the shoot-through current is limited under a designable level. Thus, there are no shoot-through concerns and the system reliability is greatly enhanced. The PWM dead-time can be minimized or eliminated. As a result, the output waveform distortion is reduced and the DC-link voltage utilization is optimized.

2) Since the high frequency loops of the dual-buck leg comprise the active switches connected in series with the external diodes. The anti-paralleled diodes of the active switches cannot be forced to turn off. In addition, their reverse currents must flow through the current limiting inductors. Thus, the recovery process here is safe. The power MOSFETs can be employed to benefit the targeted converter in terms of higher switching frequency and lower switching and conduction losses.

3) External diodes can be selected with optimized recovery characteristics and low voltage drop to reduce the switching and conduction losses.

In section 2, the topological configurations of the proposed legs are discussed. Their operating principle and competition are analyzed and compared in section 3. The practical implementation of the proposed legs for the integrated power converters is discussed in section 4. The experimental results for a single-phase dual-output inverter using the proposed legs are provided for validation.

2. Topological Configurations

Two-switch Dual-Buck Switching Circuits

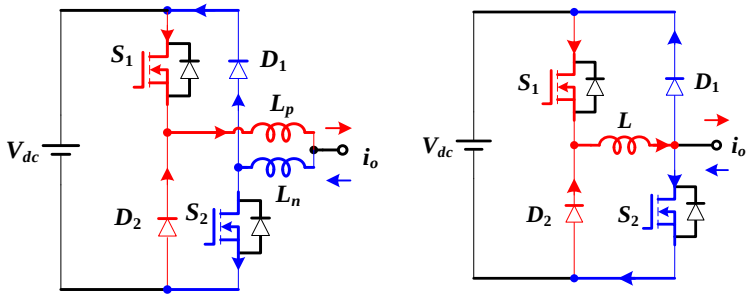


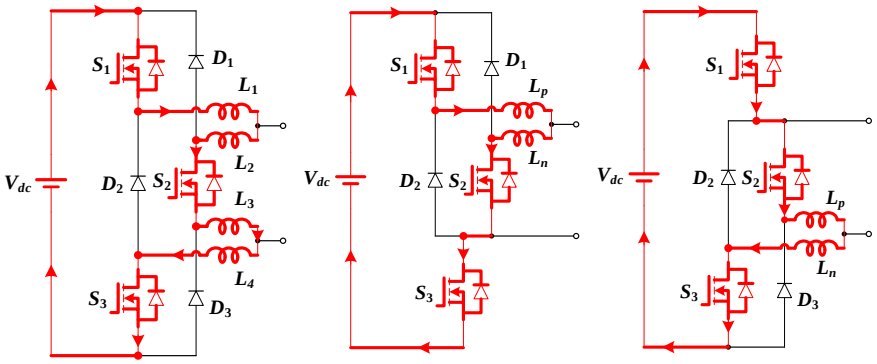
Figure 3: The dual-buck two-switch switching circuits with two (a) and one (b) current limiting inductors

The dual-buck switching circuits was first patented in 1990, to the best of our knowledge. As shown in Fig. 3, the dual-buck configuration introducing the current limiting inductors between two active switches. Thus, the dc-rail V_{dc} is prevented from short-circuit, the *dv/dt* and *di/dt* are reduced [6]. The external diodes are employed to free wheel the inductor currents, when the active switches are turned off.

Unlike the standard two-switch leg, the output current (i_o) flows in different paths depended on itsdirection. Though the structure shown in Fig. 3(b) reduces one inductor compared to the one shown in Fig. 3(a), it leads

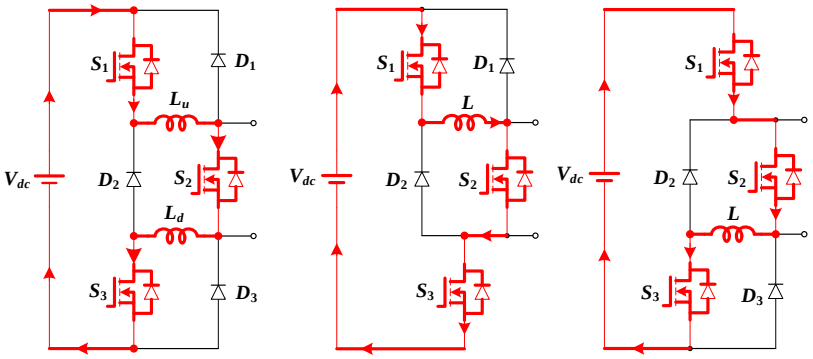
the asymmetry of the inductance introducing in the current paths. The output terminal of the one-inductor structure can be connected to either the joints of D_1 and S_2 or S_1 and D_2.

Proposed Three-Switch Dual-Buck Switching Circuits



(a) [14] (b) (c)

Figure 4: Proposed dual-buck three-switch leg configurations using two-inductor structure



(a) (b) (c)

Figure 5: Proposed dual-buck three-switch leg configurations using one-inductor structure

Like the derivation of the conventional three-switch leg, the dual-buck counterpart can also be derived by combining two dual-buck legs as shown in Fig. 4(a) [14]. Hence, there are four limiting inductors and three external diodes appearing in the circuit. Since the inductors are introduced only for limiting the *di/dt*, the limiting inductors and the external diode in the upper or lower terminal can be removed as shown in Fig. 4(b) and (c), respectively. The body diodes of S_3 and S_1respectively are employed to freewheel the output current in these proposed configurations. Owing to the presence of the limiting inductors in the shoot-through path, the *di/dt* of the reverse current is also confined. Thus, these body diodes can recover safely [6].

Similarly, by combining two one-inductor structures, the dual-buck three-switch leg with two limiting inductors and three external diodes is derived as depicted in Fig. 5(a). The one-inductor type can also be applied to the leg in Figs. 4(b) and (c). This results in two more dual-buck three-switch legs with only one current-limiting inductor and two external diodes as shown in Figs. 5(b) and (c), respectively.

In total, five novel configurations of the dual-buck three-switch leg are proposed. Owing to the current-limiting inductors existing in their shoot-through path, these legs can stand for all turned-on fault. Since, the PWM dead-time is minimized, the conduction time of body diodes can be neglected. Also, the *di/dt* of the reverse current is also limited by the limiting inductors. Therefore, there is no reverse recovery issue on the MOSFET body diodes [6].

Limiting Inductors Design

When active switches are somehow turned on or in the recovery process of the body diodes, the slew of the induced current flowing through the leg is calculated by the following equation,

$$\frac{di_c}{dt} = \frac{V_{dc} - 3V_F}{\Sigma L_c} \quad (2)$$

Where ΣL_c is the total inductance of the limiting inductors introducing to the leg, and V_F is the voltage drop on the active switches. The limiting inductors are therefore designed based on this equation so that the active switches operate within the safe area (SOA) and the protection circuits have sufficient time to handle the malfunction.

According to the above analysis, the one-inductor type configurations can only reduce the number of inductors but not the required inductance. Although, the one-inductor structured legs may cause the distortion due to the asymmetry in the current path. This issue practically can be neglected due to the fact that the inductance of the limiting inductor is commonly much smaller than those of the filter inductors. or the inductance of motor windings.

3. Operating Principle of the Proposed Legs

The conventional three-switch leg has three switching states as shown in Fig. 1(b), where for each state, there is one switch turned off and two switches turned on. When using the three-switch leg as a dual-output buck converter, there are three operating modes corresponding to switching states as shown in Fig. 6.

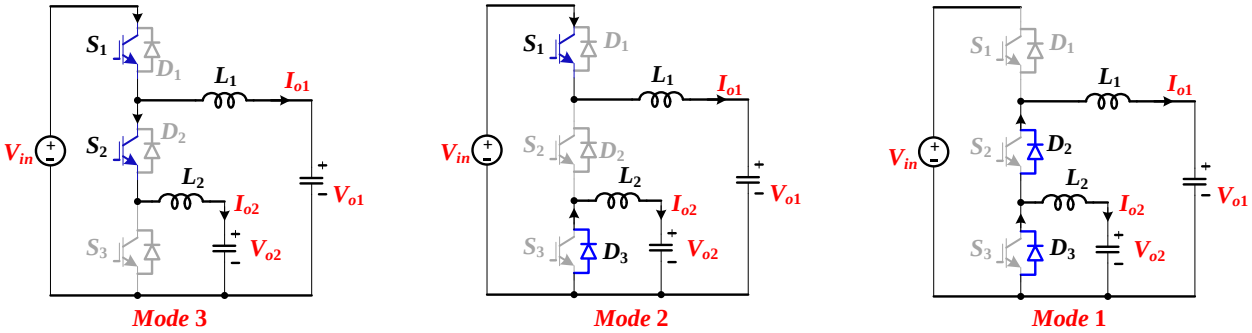
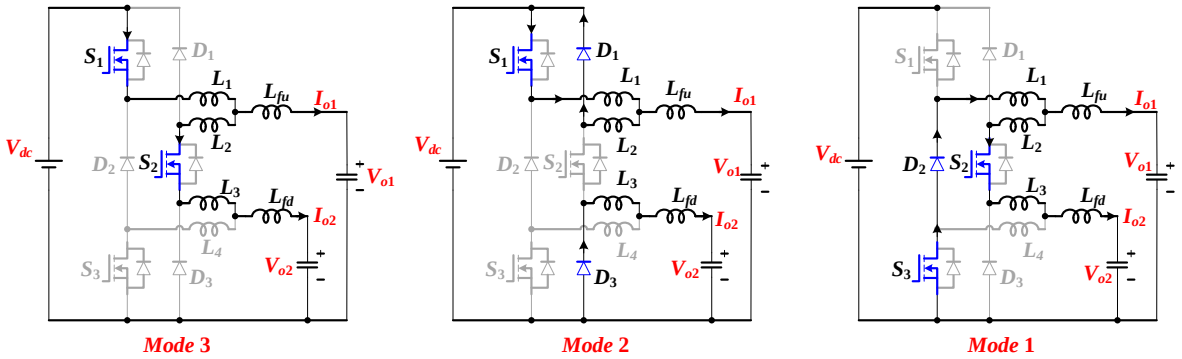
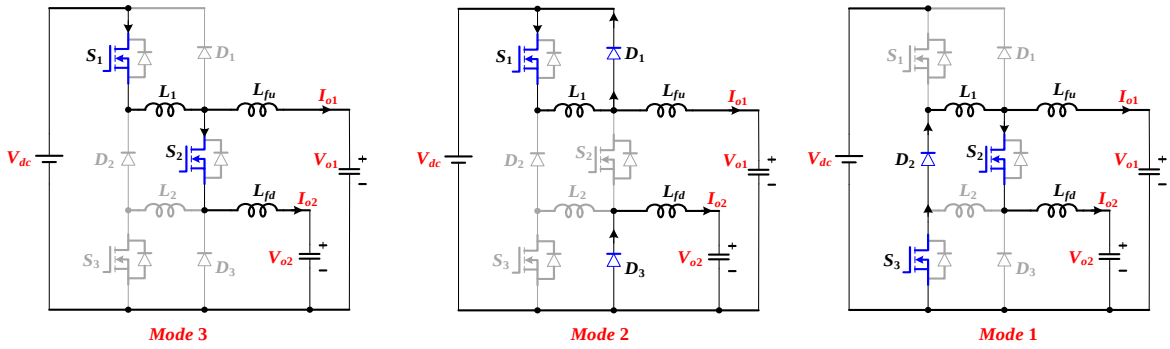


Figure 6: Operating modes of a dual-output buck converter using conventional three-switch leg

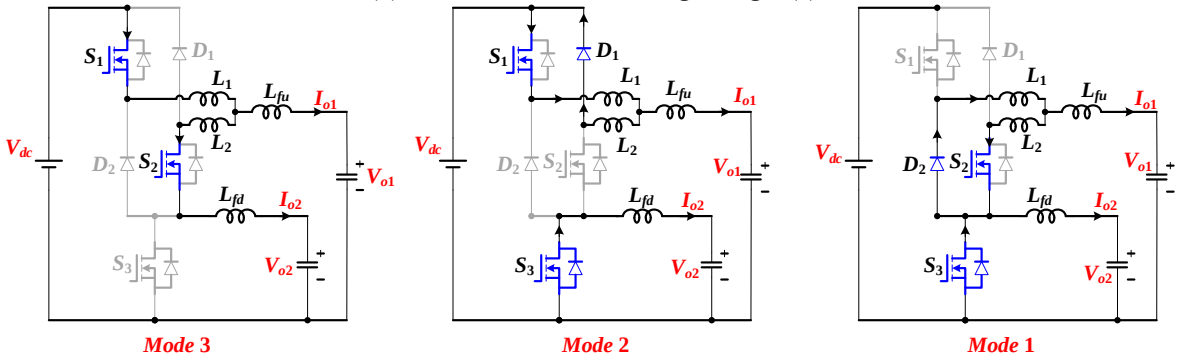
Similarly, the operating modes of the dual-output buck converters using the dual-buck three-switching legs described in Figs. 5 and 6 are shown in Fig. 7. By adding the limiting inductors, the dual-buck three-switching legs suffer from the current circulation caused by the freewheeling of the limiting inductors. For example, in the mode 2 of Fig. 7(a), the current in inductor L_2 flows through D_1, S_1, L_1 and return to L_2.



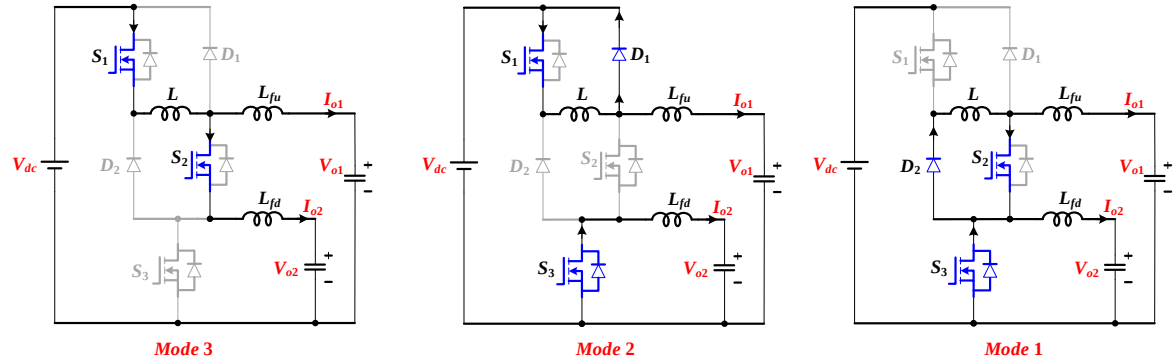
(a) dual-buck three-switch leg of Fig. 4(a)



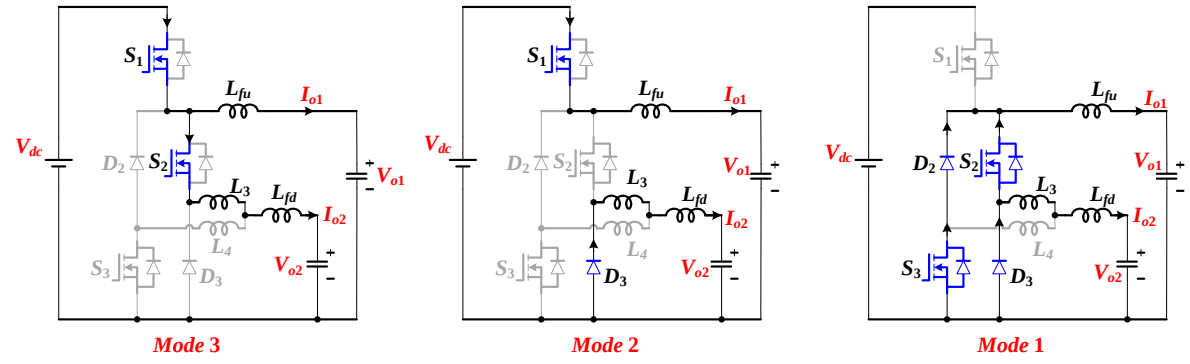
(b) dual-buck three-switch leg of Fig. 5(a)



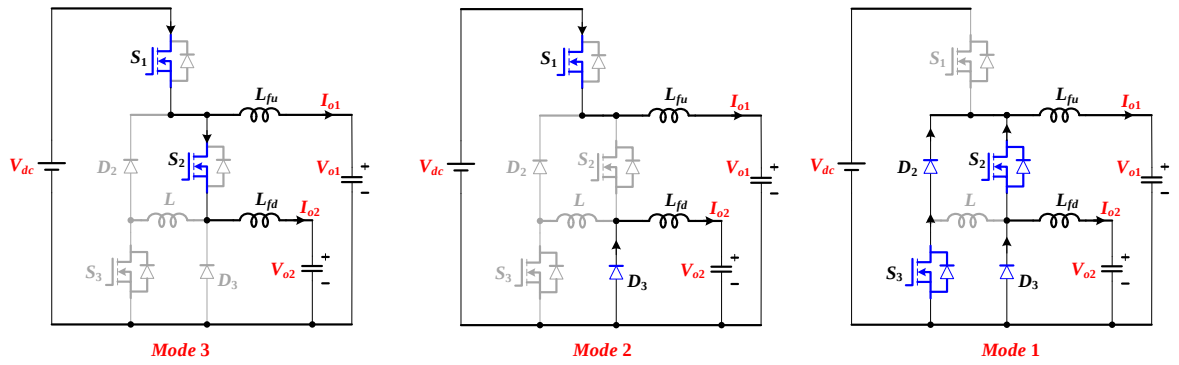
(c) dual-buck three-switch leg of Fig. 4(b)



(d) dual-buck three-switch leg of Fig. 5(b)



(e) dual-buck three-switch leg of Fig. 4(c)



(f) dual-buck three-switch leg of Fig. 5(c)

Figure 7: Operating modes of a dual-output buck converter using dual-buck three-switch leg

4. Power Loss Analysis and Comparison

The power losses in the semiconductor devices include the conduction losses, the switching losses and the blocking losses which are commonly negligible.

Conduction Losses

a) Power MOSFETs: The average conduction losses of a turned-on power MOSFET over the switching cycle is determined as [6]:

$$P_{M,c} = \frac{1}{T_s}\int_0^{T_s} R_{ds,on} i_D^2(t)dt = r_{ds,on} I_{D,rms}^2 \quad . \qquad (3)$$

Where T_s is the switching period time, $r_{ds,on}$ is the drain-source on-state resistance, i_D is the current flowing through the power MOSFET.

b) Diodes: When the power MOSFET is turned off, it blocks the drain-source current. The conduction losses in its body diode if occurs is calculated by:

$$P_{D,c} = \frac{1}{T_s}\int_0^{T_s} \left(v_{D,0} i_F(t) + R_D i_D^2(t)\right)dt = u_{D0} I_{F,av} + r_D I_{F,rms}^2 \quad . \qquad (4)$$

Where, i_F is the diode current, $v_{D,0}$ is the forward voltage when the diode current is zero, r_D the equivalent resistance of diode which is approximate by $\Delta V_D/\Delta I_F$. Similarly, the conduction losses in the anti-parallel diode of IBGT and the external diode are also determined by the above equation.

c) *IGBTs*: The collector-emitter voltage (V_{CE}) on a turned-on IGBT includes the on-state zero-current voltage ($v_{CE,0}$) and the voltage drops on the on-state resistance (r_C). Thus, the conduction losses in the IGBT is calculated as:

$$P_{T,c} = \frac{1}{T_s}\int_0^{T_s} \left(v_{CE,0} i_C(t) + R_D i_C^2(t)\right)dt = u_{D0} I_{C,av} + r_C I_{C,rms}^2 \quad . \qquad (5)$$

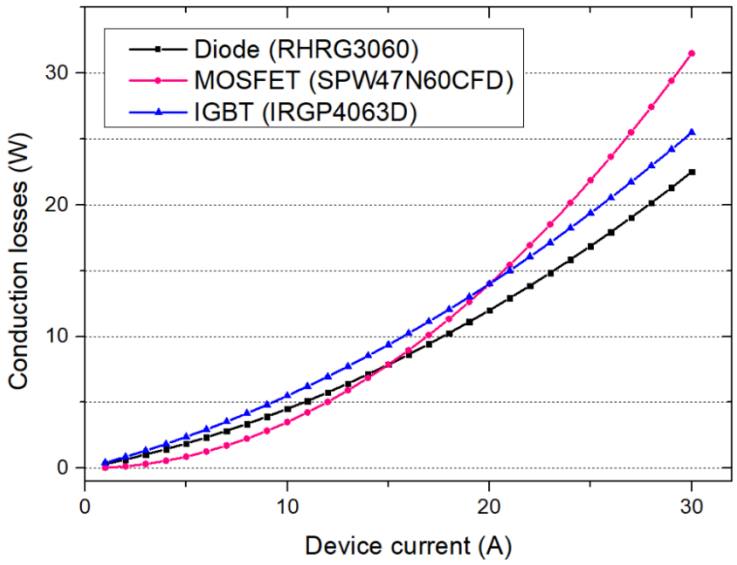


Figure 8: The comparison of the conduction losses in diode, MOSFET, and IGBT

Fig. 8 shows the comparison of the conduction losses in the power devices with 600 V rated voltage included diode (RHRG3060), MOSFET (SPW47N60CFD), and IGBT (IRGP4063D). Where the conduction time of these devices is assumed equal half of the switching period. As can be seen in the figure, the conduction loss on MOSFET is smallest when the device current is about smaller than 15 A. Excess this value, the conduction loss on MOSFET become larger than that of diode and even IGBT when the current goes over about 20 A.

Switching Losses

a) Power MOSFETs: The turn-onswitching loss in power MOSFET includes the switch-on energy itself and the loss induced by the reverse recovery of the free-wheeling diode as expressed below:

$$P_{M,on} = \left[V_{dc} I_D \frac{1}{2}(t_{ri} + t_{fu}) + E_{oss} + Q_{rr} V_{dc} \right] f_{sw} \quad (6)$$

Where f_{sw} is the switching frequency, t_{ri} is the rising time of the switch current I_D, t_{fu} is the falling time of the switch voltage, Q_{rr} is the reverse recovery charge of the free-wheeling diode, E_{oss} is the stored energy on the junction capacitorC_{oss}. The turn-off switching loss is calculated similarly with only the switch-off energy.

$$P_{M,off} = V_{dc} I_D \frac{1}{2}(t_{fi} + t_{ru}) f_{sw} \quad (7)$$

b)Diodes: When the active switch is turned on, the free-wheeling diode should be forced to turn off by the reverse-biased voltage. The reverse recovery process in the diode induce the loss which is approximate as:

$$P_{D,off} = \frac{1}{4} Q_{rr} V_{dc} f_{sw} \quad (8)$$

When the active is turned off, the free-wheeling diode is turned on the current on the inductive load. The turn-on switching loss in the free-wheeling diode is small and negligible, $P_{D,on} \sim 0$.

c) *IGBTs*: The switching loss on the IGBTs can be calculated by the turn-on and turn-off energies (E_{on} and E_{off}) provided in the datasheet:

$$P_{T,on} = E_{on} f_{sw}; \quad P_{T,off} = E_{off} f_{sw} \quad (9)$$

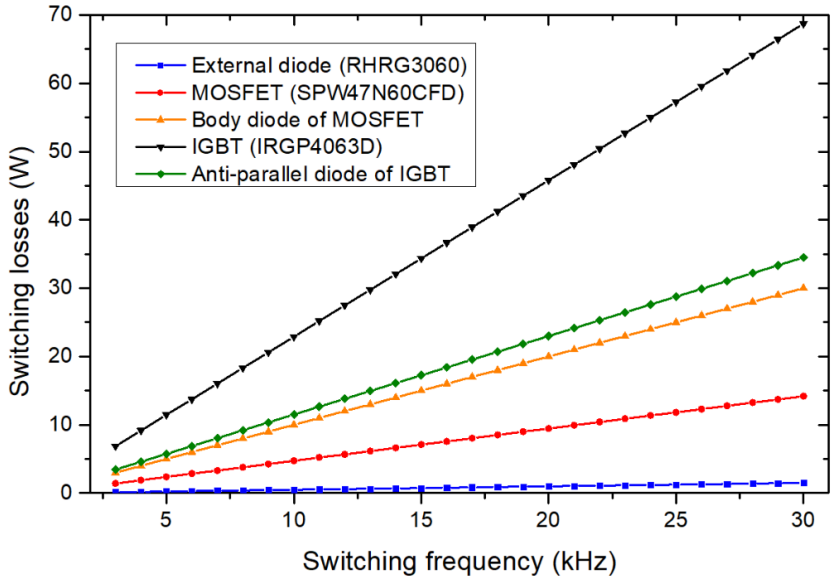


Figure 9: The comparison of switching losses induced by the transition of diodes, MOSFET, and IGBT

The switching losses induced by MOSFET, IGBT, theirs accompanying diodes, and external diode is compared in Fig. 9. As can be seen, the MOSFET induces much smaller losses than IGBTs and the switching losses caused by external diode is negligible compared to the anti-parallel diode of MOSFET and IGBT. Where the parameters of the switch voltage V_{dc} and current I_D are 400 V and 20 A, respectively.

Since the transition of an active switch always associates with that of a freewheeling diode, the combination of a MOSFET and an external diode induces the smallest total switching losses.

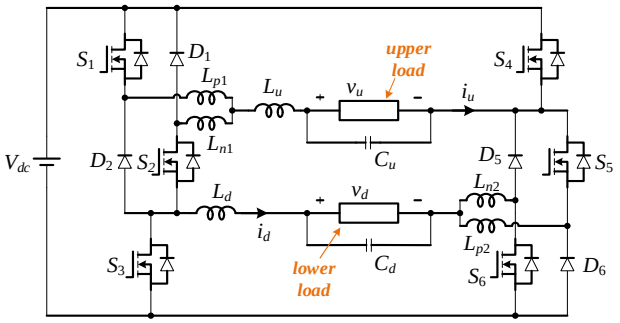


Figure 10: Dual-buck three-switch leg configurations using one-inductor type structure

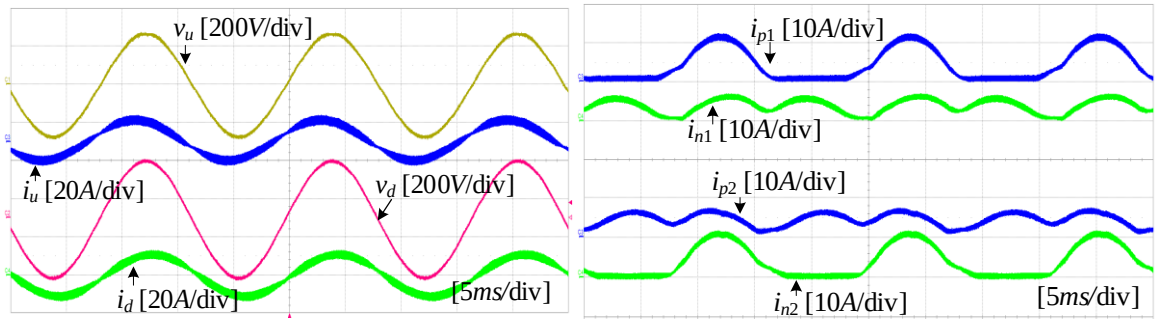
Table 2: Experimental Parameters

Input voltage (V_{dc})	400 V
Switching frequency (f_{sw})	30 *k*Hz
MOSFET ($S_{1\text{-}6}$)	47N60CFD
Diode ($D_{1\text{-}2,5\text{-}6}$)	RHRG3060
Limiting inductors ($L_{p1\text{-}2}$, $L_{n1\text{-}2}$)	0.2 *m*H
Filter inductors ($L_{u,d}$)	0.74 *m*H
Filter capacitors ($C_{u,d}$)	6 *μ*F

5. Experimental Verification

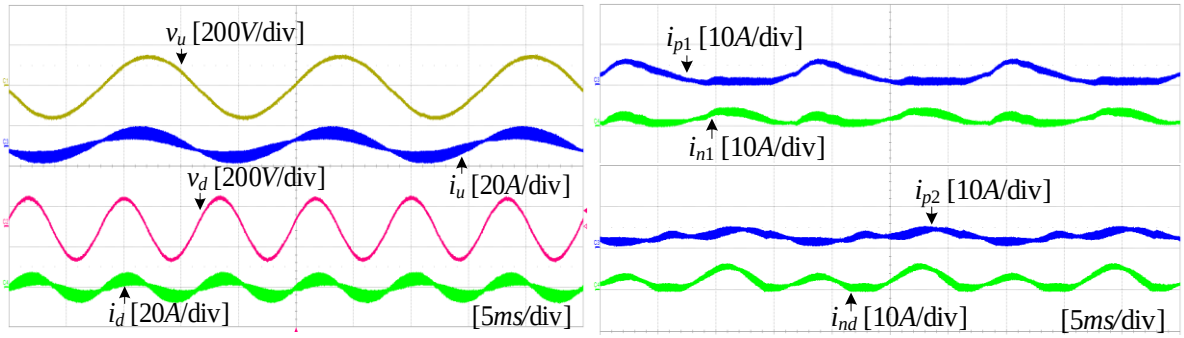
To verify the practicability, the dual-buck three-switch legs in Figs. 5(b) and (c) are used to build a single-phase dual-out inverter, as shown in Fig. 10, where the inductors (L_u, L_d) and capacitors (C_u, C_d) function as the filters for the upper and lower loads. A hardware prototype of this inverter is fabricated using the experimental parameters in Table II. The upper load consists of a 50-Ω resistor in series with a 200-μF capacitor, while the lower load is inductive with a 50-Ω resistor and a 50-mH inductor connected in series. The operation and PWM

control strategy of this dual-output inverter are the same as those of the conventional one in [15] or the dual-buck one in [14].



(a) (b)

Figure 11: Experimental results in CF mode. (a) Output voltage and current waveforms. (b) Limiting inductor current waveforms



(a) (b)

Figure 12: Experimental results in DF mode. (a) Output voltage and current waveforms. (b) Limiting inductor current waveforms

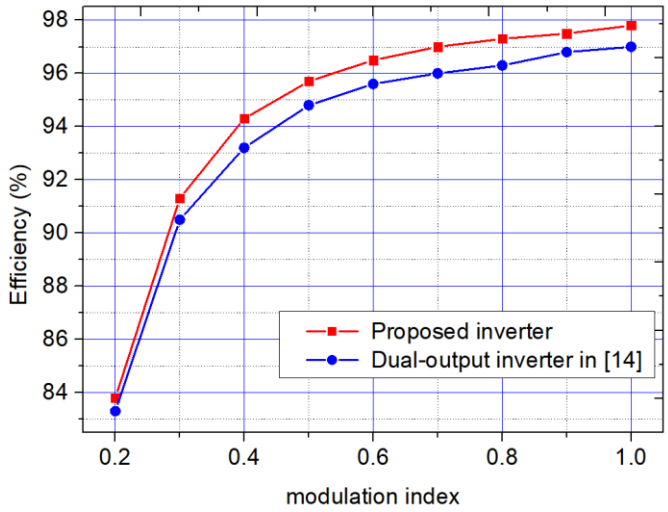


Figure 13: Efficiency comparison

Fig. 11 shows the experimental results in the common-frequency (CF) mode, where the additional offsets are ±0.06, the modulation indices are m_u= 0.7, m_d = 0.8, and the fundamental frequencies of both outputs are 60 Hz. The experimental results in the different-frequency (DF) mode are shown in Fig. 12, where the modulation indices of m_u = 0.4, m_d = 0.45, the additional offsets of ±0.25 are used, and the fundamental frequencies of the upper and lower outputs are 60 Hz and 120 Hz, respectively. Where, i_{p1}, i_{n1}, i_{p2}, and i_{n2} represent the currents in the limiting inductors L_{p1}, L_{n1}, L_{p2}, and L_{n2}, respectively. As is evident in the figures, two outputs are decoupled and can operate independently under either the CF or DF mode.

In Fig. 13, the efficiency of the proposed inverter, which uses the dual-buck three-switch legs in Fig. 5(b) and (c), is compared with the dual-output inverter in [14-15], which uses the dual-buck three-switch legs in Fig. 5(a). Owing to the reduction in passive components, the proposed inverter achieves higher efficiency and peaks at 97.8%.

6. Conclusions

Following the trend of extending the dual-buck structure to the three-switch leg, this letter proposed a family of improved dual-buck three-switch legs using minimal numbers of limiting inductors and external diodes. This reduces the cost, size, and weight of the converter system. The proposed dual-buck three-switch legs can equally replace the conventional three-switch leg in the reduced-switch-count converters to obtain a higher efficiency and a higher switching frequency using power MOSFETs. The system reliability is also greatly improved owing to no shoot-through concerns.

Acknowledgments

We acknowledge the support of time and facilities from both Ho Chi Minh City University of Technology (HCMUT), VNU-HCM, and Clarkson University for this study.

References

[1]. Kominami, T. and Fujimoto, Y. (2007). A novel nine-switch inverter for independent control of two three-phase loads. *Proc. IEEE IAS*, pp. 2346–2350.

[2]. Liu, C., Wu, B., Zargari, N. R., Xu, D., and Wang, J. (2009). A novel three phase three-leg ac/ac converter using nine IGBTs. *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1151–1160.

[3]. Qin, Z., Loh, P. C., and Blaabjerg, F. (2014). Power loss benchmark of nine-switch converters in three-phase online-ups application. *Conf. Rec. IEEE ECCE 2014*, pp. 1180-1187.

[4]. Loh, P. C., Zhang, L., and Gao, F. (2013). Compact integrated energy systems for distributed generation. *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1492-1502.

[5]. Mahdi Azizi, Mustafa Mohamadian, and Reza Beiranvand (2016). A new family of multi-input converters based on three switches leg. *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6812-6822.

[6]. Huang, A. (2014). Hard commutation of power MOSFET OptiMOS FD 200V/250V. *Application Note AN201403*. Infineon, Neubiberg, Germany, pp. 1–13.

[7]. Chen, L., and Peng, F. Z. (2008). Dead-time elimination for voltage source inverters. *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 574-580.

[8]. Yao, Z., Xiao, L., and Yan, Y. (2009). Control strategy for series and parallel output dual-buck half bridge inverters based on DSP control. *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 434–444.

[9]. Shin, H., Cha, H., Kim, H., and Yoo, D. (2015). Novel Single-Phase PWM AC-AC Converters Solving Commutation Problem Using Switching Cell Structure and Coupled Inductor. *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2137-2147.

[10]. Sun, P., Liu, C., Lai, J.S., Chen, C.L., and Kees, N. (2012). Three-phase dual-buck inverter with unified pulse width modulation. *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1159-1167.

[11]. Peng-wei, S., Chuang, L., and Jih-Sheng, L. "Cascade (2012). Dual buck inverter with phase-shift control. *IEEE Trans. Power Electron*., vol. 27, no. 4, pp. 2067-2077.

[12]. Sun, P., Liu, C., Lai, J.S., Chen, C.L., and Kees, N. (2012). Three-phase dual-buck inverter with unified pulse width modulation. *IEEE Trans. Power Electron*., vol. 27, no. 3, pp. 1159–1167.

[13]. Chen, B., et al. (2015). A high-efficiency MOSFET transformerless inverter for nonisolated micro-inverter applications. *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3610–3622.

[14]. Nguyen, B., Cha, H., and Kim, H. (2018). Single-Phase Six-Switch Dual-Output Inverter Using Dual-Buck Structure. *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp.7894 - 7903.

[15]. Fatemi, A., Azizi, M., Mohamadian, M., Varjani, A.Y., and Shahparasti, M. (2013). Single-phase dual-output inverters with three-switch legs. *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1769-1779.