Available online www.jsaer.com

***Journal of Scientific and Engineering Research*, 2024, 11(3):312-316**

Research Article

ISSN: 2394-2630
CODEN(USA): JSERBR

Handset Camera Processor with Advanced Sensor Low Noise Model

Apoorva Reddy Proddutoori

San Diego
apoorvaproddutoori@gmail.com

Abstract: This paper presents an energy-efficient, illumination-adaptive camera sensor processor for distributed digital sensor applications. This adaptive feature allows for continuous imaging operations with minimal power consumption, extending the lifespan of wireless sensor nodes and delivering optimal image quality across a broad spectrum of illuminations. The sensor utilizes configurable operating modes, primarily in a monitoring mode that maintains low power usage for extended operation. It transitions to high-sensitivity or wide dynamic range imaging modes in response to changes in illumination and sufficient energy availability from energy harvesting. The photoluminescence imaging technique has recently gained recognition for its effectiveness in rapidly sorting silicon-based solar wafers and cells. In this study, we present a cost-effective photoluminescence imaging system, focusing on its various components. The sensor then returns to the monitoring mode to conserve battery energy. In the monitoring mode, the sensor operates at a low-power level, enabling it to capture high-resolution and wide dynamic range images from sensor energy. The device achieved a power-on-mode (POM) of in technology.

Keywords: camera, sensor, performance, imaging, power, energy

Introduction

The development of a low-voltage and power-efficient image sensor for emerging applications in implantable biomedical devices and wireless sensor networks has emerged as a significant area of research. The increasing demand for CMOS Camera sensor (CCS) technology, driven by its low-power operation and high system integration capabilities, is expected to continue.

For portable devices and mobile imaging, power-saving techniques are employed to prolong usage time, especially under battery constraints. In the biomedical field, where implantable and disposable devices are common, ultra-low-power design is crucial. To reduce power consumption in CCS, the primary challenges include developing low-voltage, low-leakage, and power-efficient techniques. In the last decade, there has been a surge in research on new architectures for the implementation of CMOS image sensor technology, aiming to gain an economic edge in the competitive solid-state image sensor market. With the advent of deep nanometer CMOS processors, it is now feasible to create high-performance single-chip cameras capable of integrating image capture with advanced on-chip computational circuitry. The low voltage swing, a characteristic of visual sensory processors like the CMOS active pixel sensor (APS) designs, has led to reduced signal-to-noise ratio (SNR) and a diminished dynamic range. The smallest achievable pixel size is limited by imaging optics and light aliasing factors. Applications of computational photography, such as light field photography, enable the capture and synthesis of images that traditional cameras cannot. Non-linear filtering techniques, like bilateral filtering, play a crucial role in computational photography. These techniques have a broad range of applications, including High-Dynamic Range (HDR) imaging, Low-Light Enhanced (LLE) imaging, tone management, and

video enhancement. The high computational complexity of multimedia processing applications necessitates the development of fast hardware implementations to support real-time processing.

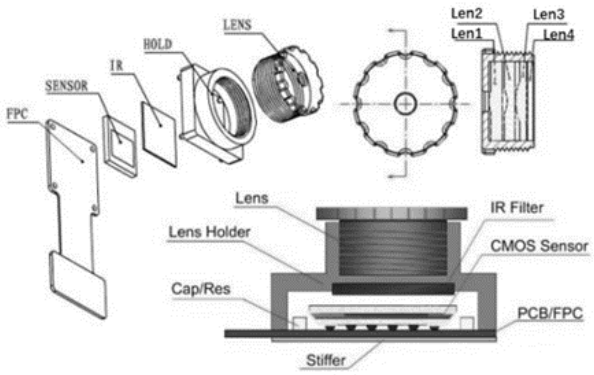

Figure 1: Camera Sensor Architecture

Low-power, low-cost, miniature, and integrated digital imaging systems are poised to become ubiquitous in consumer electronics in the near future. However, until recently, video technology had largely been excluded from the mainstream of CMOS VLSI, with the prevailing imaging technology being charge-coupled devices. The dominance of CCS was attributed to their superior sensitivity, dynamic range, uniformity, low noise, and small pixel size. Yet, CCS necessitate specialized silicon processing that is not compatible with CMOS technology. Moreover, CCS are high- capacitance devices, requiring multiple non-standard and high-voltage clocks and biases, and they provide only serial output (random access is not supported). The high device capacitance, large clock swing, need for DC-DC converters, and the inability to integrate control and processing electronics on the imaging chip contribute to the bulkiness and power consumption of CCS-based imaging systems.

CMOS Camera Sensor

The original process relied on a conventional and manually crafted computer vision algorithm (CVA), which was highly accurate but only effective under stable light conditions. This was primarily due to the CVA's methodology, which involved calculating derivatives from the input image, which required significant contrast. To mitigate this sensitivity to light conditions, the process introduced a variable acquisition time for the camera, allowing it to adapt to different lighting conditions for clear image capture. However, this adjustment compromised the vehicle's agility due to the variability and length of the acquisition time. To address these limitations, we took an AI-based approach with the goal of replacing the CVA with a Convolutional Neural Network (CNN). The objectives were to enhance the algorithm's robustness to changes in lighting conditions and to boost its performance, specifically in terms of actions per second, by learning complex features from short yet continuous acquisition periods.

In traditional CMOS active pixel sensors (APS) pixels, the photo-generated charge is converted into voltage and read out through a voltage buffer, which is usually achieved through a source follower circuit. The input-output voltage drop of this source follower circuit reduces the range of available signal swing at the conversion node and also limits the sensor's full-well capacity. To overcome these challenges associated with full-well limitations at ultra-low voltage operations and to extend the dynamic range, a pulse-width modulation (PWM) image sensor was proposed as an effective solution. Instead of utilizing a conventional APS pixel, the PWM sensor converts the photo-generated voltage signal into a pulse width across the pixel and readout in digital form. This approach not only bypasses the need for a significant voltage headroom provided by analog buffers but also efficiently avoids the degradation of full-well capacity that typically occurs with a decrease in voltage operation.

The conventional approach to micro-photoluminescence systems involves acquiring the photo-generated light signal point by point, sweeping the excitation beam across the sample. Such systems, characterized by high-performance optics and detectors, are capable of capturing high-quality photoluminescence (PL) images. However, their complexity, cost, and time required to complete an experiment often exceed the standards for an

in-line tool. In contrast, the photoluminescence imaging technique collects the whole luminescence signal from the entire area being explored in a relatively short time (milliseconds to a few seconds). This capability is achieved by illuminating the entire sample and using highly efficient CCD camera detectors to capture the photo-generated light signal.

Operating at the maximum sensitivity constantly consumes a significant amount of power, rendering it impractical for energy-constrained applications. Additionally, it is not feasible to simultaneously optimize the sensitivity and dynamic range for capturing images under a broad spectrum of illumination conditions. Thus, there is a critical need for an image sensor that is adaptable to varying energy availability and light conditions. Our approach involves designing an energy-vigilant CMOS image sensor capable of operating in four different modes: monitoring, normal, high sensitivity, and wide-dynamic-range (WDR) modes. In this paper, we introduce our design and its benefits.

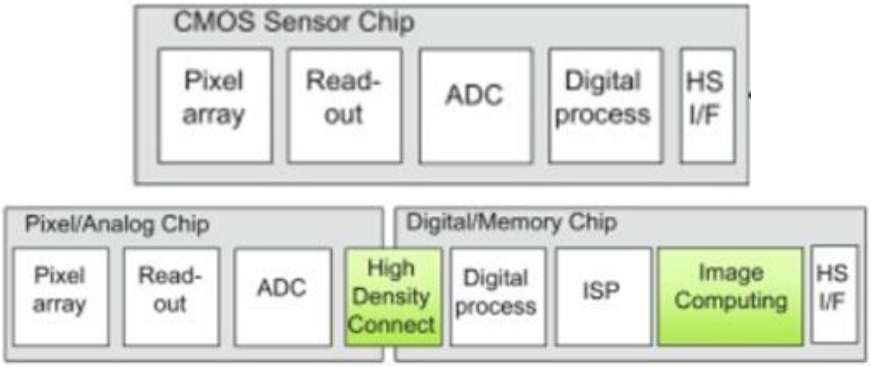

Figure 2: CMOS Sensor Processor

Although it may appear to be straightforward, collecting data from sensors can have an impact on the construction process and the design of an application. For instance, if the images aren't clear or take too long to process, quickly taking in raw images can make the system slower or overburden its memory. When multiple sensors are used, it may be necessary to combine their data into one. It's possible that this additional work will occur concurrently with the rest of the app, making it less effective. Utilizing various components of the system, such as a DSP, is another option; however, this comes with its own set of difficulties, including the additional steps required to ensure that everything functions properly. We discovered that some apps took a long time to run because of the data handling code.

Using cutting-edge CMOS technology and a novel architecture, our goal is to put the fundamental learning principles that have been observed in biological nervous systems into practice in this observation. Utilizing digital logic and memory circuits in the creation of neuromorphic processors is our primary focus. Through transistor scaling and dynamic voltage scaling, respectively, these circuits are able to produce hardware that is both dense and low-power, which makes them advantageous. For use in data clustering and pattern recognition, we will demonstrate two neuromorphic processors with integrate-and-fire neurons and plastic synapses.

Sensor's Photo-Electronics Processing

The operation of photoelectrons is best detected by a small integration capacitor. However, getting just a few electrons to move from a large photodiode capacitor within a brief time is a daunting task. The conventional lateral transfer gate method faces this challenge head-on. Here, a small voltage change on the photodiode generates a minuscule transfer current that, in turn, takes an extensive period to settle and complete the charge transfer. Consequently, this leads to image lag, especially with weak illumination.

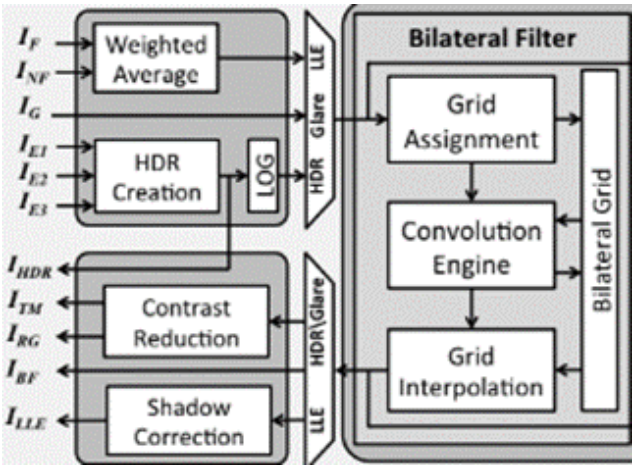

Figure 3: Temporal Filter

Designing an in-pixel comparator is crucial for PWM CIS, which demands it to be both straightforward and uniform. To achieve simplicity and a high fill factor, the inverter-based comparator is the preferred choice. However, this approach's sensitivity to process variation results in a non-uniform response across the pixel array. We propose a solution that cancels threshold variation to eliminate fixed pattern noise in PWM CIS. Additionally, we suggest a programmable current-controlled threshold to achieve an impressive dynamic range at a supply voltage of 0.65 V.

Applications that require on-chip autonomous wireless security cameras, disposable medical imaging systems, and similar devices are turning to technologies capable of operating under low voltage, consuming minimal power, and being compatible with deep nanometer processes. Hence, the use of the more conventional array of parallel switches (APS) is giving way to the popular PWM imaging approach, which overcomes the challenges of limited signal swing seen under low-voltage operation (achieved with 1.35 V supply voltage) with dynamic pixel-by-pixel have developed a threshold variation noise-canceling scheme that boasts an impressive dynamic range at 0.65 V supply voltage and consumes just under the same conditions.

The approach employs an in-pixel two-transistor comparator with a column-shared current limiter, achieving a signal-to-noise ratio (SNR) at a supply voltage of 0.65 V and a power consumption of just <mW. Nonetheless, achieving ultra-low power consumption demands careful supply voltage scaling and the introduction of control techniques that, in turn, restrict the frame rate. This approach is vulnerable to variations in supply voltage.

In digital still imaging or slow-scan imaging, exposure times can span from a mere 70 microseconds to incredibly long. To manage this, our imager operates with a unique two-pointer addressing scheme. A pointer, defined as a decoded row address, initiates the integration for a row, followed by a row read sequence. Thus, the exposure time is determined by the timing between these integration and readout pointers for a specific row. Since the integration and readout of different rows are interleaved, a typical row cycle is composed of four sub-cycles: initiation of integration for row m, pixel readout for row m-k, parallel digitization of the row, and digital data output.

Conclusion

The proposed Time-to-Threshold (PWM) VLSI architecture, developed using conventional CMOS technology, has demonstrated significant potential in terms of robustness, high fill factor, favorable signal-to-noise ratio, and the capability to operate as low as 400 mV.

The output of the inverter, and thus the readout, is mapped onto a variable-width digital pulse based on the intensity of the incident light. This architecture offers different pulse widths that are directly related to the luminance level, rather than the number of reset events, when compared to existing methods.

The design of the pixel circuit is meticulous to minimize Optical Transient Assumed Noise (OTA) and the impact of leakage currents. Moreover, an on-chip calibration system is implemented to offset any discrepancies in the MOS capacitor's magnitude.

References

[1]. Rahul Rithe, Priyanka Raina, Nathan Ickes, Srikanth V. Tenneti Anantha P. Chandrakasan, "Reconfigurable Processor for Energy-Scalable Computational Photography", ISSCC 2013 / SESSION 9 / MOBILE APPLICATION PROCESSORS AND MEDIA ACCELERATORS

[2]. Bedabrata Pain, Guang Yang, Monico Ortiz, Kenneth McCarty, Bruce Hancock, Julie Heynssens, Thomas Cunningham, Chris Wrigley, & Charlie Ho, "A Single-chip Programmable Digital CMOS Imager with Enhanced Low-light Detection Capability", IEEE

[3]. Kyoungrok Cho, Omid Kavehei, "High Fill Factor Low-Voltage CMOS Image Sensor Based on Time-to-Threshold PWM VLSI Architecture" IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 7, JULY 2014

[4]. Miguel de Prado, Manuele Rusci, Romain, Alessandro Capotondi, Serge Monnerat, Luca Benini, Nuria Pazos, "Robustifying the Deployment of tinyML Models for Autonomous mini-vehicles", 2021 IEEE International Symposium on Circuits and Systems (ISCAS)

[5]. Jaehyuk Choi, Seokjun Park, Jihyun Cho, and Euisik Yoon, "An Energy/Illumination-Adaptive CMOS Image Sensor with Reconfigurable Modes of Operations", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 50, NO. 6, JUNE 2015

[6]. B. Moralejo*, A. Tejero, O. Martínez, M. A. González, J. Jiménez, "Low-Cost system for full-wafer photoluminescence characterization of photovoltaic silicon", IEEE